having an output at which a downstream and upstream clock signal generated from said master clock signal appears, each of said upstream and downstream clock signals being phase coherent with said master clock signal;

a downstream data input;

an SCDMA downstream modulator coupled to said downstream data input and coupled to receive said downstream clock signal and having a chips output;

a downstream carrier synthesizer coupled to receive said master clock signal and having a downstream carrier output at which a downstream carrier appears which is phase coherent with said master clock signal;

a first mixer having a first input coupled to said chips output and having a second input coupled to said downstream carrier output and having an output at which modulated downstream signals appear for coupling to a transmission media or media transmitter;

a second mixer having an input for coupling to a transmission medium or media receiver, and having a carrier input for receiving an upstream carrier, and having an output at which baseband demodulated upstream signals appear;

an upstream carrier synthesizer coupled to receive said master clock signal and having an output at which a synthesized upstream carrier signal appears which is phase coherent with said master clock signal, said output coupled to said carrier input of said second mixer; and

an SCDMA upstream demodulator having an input coupled to said output of said second mixer and having an input coupled to receive said upstream clock signal, and having an output at which recovered upstream data appears, and including means for correcting phase and amplitude errors in incoming

constellation points transmitted from other data transmission nodes located at varying distances from said data transceiver, and further comprising means for achieving frame synchronization or minislot boundary synchronization.

2. (Amended) A digital data transceiver comprising:

a first mixer having an input for receiving code division multiplexed downstream signals and having a carrier input for receiving a local downstream carrier, and having a product output at which demodulated signals appear;

an SCDMA demodulator having an input coupled to said product output and having a clock input and having a clock steering output and having a recovered downstream data output;

a voltage controlled oscillator having an error signal input coupled to said clock steering output and having a recovered clock output;

a clock multiplier having an input coupled to said recovered clock output and having a recovered downstream clock output coupled to said clock input of said SCDMA demodulator;

a clock divider having an input coupled to said recovered clock output and having [an] a clock output;

a first synthesizer having an input coupled to said clock output of said clock divider and having an output coupled to said carrier input of said first mixer at which a first carrier appears which is phase coherent with said recovered clock;

an SCDMA modulator/multiplexer having an input for receiving upstream data and having a clock input coupled to said recovered clock output of said clock

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multiplier and, optionally, capable of carrying out any form of prior art ranging or other process to achieve frame synchronization or alignment of minislot boundaries of said data transceiver with minislot boundaries in a receiving node, and if said ranging or other prior art process to achieve frame synchronization or alignment of upstream minislot boundaries with minislot boundaries at a receiving node are carried out externally to said SCDMA modulator/multiplexer, said SCDMA modulator/multiplexer also has an input for receiving a transmit frame timing delay value derived by said conventional ranging or other prior art processes to achieve frame synchronization or alignment with minislot boundaries, said transmit frame timing delay value for use in setting the proper transmit timing delay to achieve frame synchronization or minislot boundary alignment at a receiving node with like numbered frames or minislots transmitted from other data transceivers transmitting to the same receiving node from different locations, and having an output at which code division multiplexed upstream signals appear;

a second synthesizer having a clock input coupled to said clock output of said clock divider and having an upstream carrier output at which an upstream carrier appears which is phase coherent with said recovered clock;

a second mixer having an input coupled to said output of said SCDMA modulator and having an input coupled to said upstream carrier output of said second synthesizer, and having an output for coupling to a shared transmission media.

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3. (Amended) A digital data transceiver comprising:

a master clock for generating a master downstream clock signal at a clock output having a frequency which is an integer multiple of a downstream symbol or chip rate, F_{ds};

a downstream modulator implementing any form of TDMA or CDMA multiplexing or no multiplexing at all and any form of modulation, and having a clock input coupled to said clock output of said master clock, and having a data input for receiving downstream data and having a data output at which symbols to be transmitted downstream appear;

a downstream mixer having a data input coupled to said data output of said downstream modulator and having a carrier input for receiving a downstream carrier, and having a data output for coupling to a transmission media;

an upstream clock generator having a clock input coupled to said clock output of said master clock and having an upstream clock output at which appears an upstream clock signal having a frequency which is M/N times the frequency of said downstream clock signal where M and N are integers;

a frequency divider having a clock input coupled to said upstream clock output of said [master clock] upstream clock generator and having a carrier clock output at which a carrier clock signal appears;

a downstream carrier synthesizer coupled to receive said carrier clock signal from said frequency divider and having an output at which appears a downstream carrier signal which is phase coherent with said downstream clock signal and which is coupled to said carrier input of said downstream mixer;

an upstream carrier synthesizer having a clock input coupled to said carrier clock output of said frequency divider, and having an upstream carrier output at which appears an upstream carrier signal which is phase coherent with said master downstream clock signal;

an upstream mixer having a carrier input coupled to said upstream carrier output of said upstream carrier synthesizer, and having an input for coupling to a transmission media to receive upstream signals, and having an output at which baseband demodulated upstream signals appear;

an upstream demodulator/demultiplexer implementing any form of TDMA or SCDMA or CDMA demultiplexing, or no demultiplexing at all if the incoming data is not multiplexed, and which implements any form of demodulation, and which is capable of carrying out prior art ranging or other processes to achieve frame synchronization or alignment of minislot boundaries of the transmitted signal to minislot boundaries in said data transceiver, and having a clock input [for receiving said upstream clock signal] coupled to said clock output of said master clock, said upstream demodulator/demultiplexer having an input [and] coupled to receive said baseband demodulated upstream signals, and having an output at which appears recovered upstream data.

4. (Amended) A data transceiver, comprising:

a downstream mixer having an input for coupling to a transmission media and having a downstream carrier input, and having an output at which baseband downstream signals appear;

a downstream demodulator/demultiplexer which can be any conventional

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demodulator/demultiplexer and which has [an] a clock input to receive a downstream clock signal and an input coupled to receive said baseband downstream signals, and an output at which recovered downstream data appears and which includes conventional downstream clock recovery circuitry, and a clock steering output at which appears a clock steering signal;

a voltage controlled oscillator having a control input coupled to [receive] said clock steering output so as to receive said clock steering signal, and having a recovered downstream clock output at which a recovered downstream clock signal appears, said downstream clock output coupled to said clock input of said downstream demodulator/demultiplexer;

an upstream clock generator having an input coupled to receive said recovered downstream clock signal and having an upstream clock output at which appears an upstream clock signal which is phase coherent with said recovered downstream clock signal and which has a frequency which is related to the frequency of said downstream clock signal by the ratio M/N where M and N are integers;

a frequency divider having a clock input coupled to said upstream clock output so as to receive said upstream clock signal, and having a carrier clock output at which a carrier clock signal appears;

a downstream carrier synthesizer having a clock input coupled to said carrier clock output to receive said carrier clock signal, and having a downstream carrier output at which a downstream carrier appears which is phase coherent with said recovered downstream clock, said downstream carrier output coupled to said downstream carrier input of said downstream mixer;

an upstream carrier synthesizer having a clock input coupled to said carrier clock output to receive said carrier clock signal, and having an upstream carrier output at which an upstream carrier signal appears which is phase coherent with said recovered downstream clock;

an upstream mixer having an upstream carrier input coupled to said upstream carrier output and having a symbol input for receiving symbols to be transmitted upstream, and having an output for coupling to a transmission media; and

an upstream modulator/multiplexer which is capable of performing one or more forms of multiplexing including TDMA or SCDMA or CDMA [multiplexing] using any prior art circuitry and is, optionally, capable of carrying out ranging or other prior art processes of achieving frame synchronization or alignment of upstream minislot boundaries with minislot boundaries at a receiving node, and having an input coupled to said upstream clock output and having an input for receiving upstream data and, if said ranging or other prior art process to achieve frame synchronization or alignment of upstream minislot boundaries with minislot boundaries at a receiving node are carried out externally to said upstream modulator/multiplixer, said upstream modulator/multiplexer also has [having] an input for receiving a transmit frame timing delay value derived by said conventional ranging or other prior art processes to achieve frame synchronization or alignment with minislot boundaries for use in setting the proper transmit timing delay to achieve frame synchronization or minislot boundary alignment at a receiving node with like numbered frames or minislots transmitted from other data transceivers

transmitting to the same receiving node, and having an output coupled to said symbol input of said upstream mixer.

5. (Amended) A digital data communication system comprising:

a shared transmission medium;

in a first node:

a master clock for generating a downstream clock signal having a frequency F_{DS};

a first upstream clock generation means having an input coupled to receive said downstream clock signal from said master clock for generating at an output an upstream clock signal having a frequency F_{US} which has a frequency equal to $(M/N)*F_{DS}$ where M and N are integers;

first means having an input for receiving downstream data to be transmitted on said shared transmission media and having an input coupled to receive said downstream clock signal, and having an output coupled to said shared transmission medium, for generating a downstream carrier from said downstream clock signal and using said downstream clock signal to organize said downstream data into a plurality of symbols, and, if necessary, using said downstream clock signal to time division or code division multiplex said symbols if data from more than one sources must be kept separate, and modulating said symbols onto said downstream carrier and launching the modulated downstream signals into said shared transmission medium;

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in one or more second nodes:

second means having an input coupled to said shared transmission media and having clock recovery means for recovering said downstream clock signal from modulated downstream signals on said shared transmission media and outputting the recovered downstream clock signal at a dowstream clock output, said second means functioning to use said recovered downstream clock signal to demodulate said modulated downsteam signals and recover said downstream data or, if necessary, to demultiplex said demodulated downstream signals to generate demultiplexed signals and recover said downstream data from said demultiplexed signals;

a second upstream clock generation means having an input coupled to receive said recovered downstream clock and having an output at which [said] a phase lock loop generates an upstream clock signal having a frequency $F_{US} = (M/N)*F_{DS}$ where M and N are integers, said upstream clock signal being generated from said recovered downstream clock signal so as to be phase coherent with said recovered downstream clock signal;

third means having an input for receiving upstream data bits and having an input coupled to receive said upstream clock signal, said third means for using said upstream clock signal to organize said upstream data bits into one or more chips or symbols to be transmitted to said first node, and, if necessary, for using said upstream clock signal to multiplex said chips or symbols of upstream data from different sources using time

division or code division multiplexing into a plurality of timeslots or result vectors to be transmitted, and for generating a phase coherent upstream carrier from said upstream clock signal, and for modulating said timeslots or result vectors of upstream data onto said upstream carrier to generate upstream signals and launching said upstream signals into said shared transmission medium and translating the frequency of the upstream signals to a selected frequency in [the] an upstream band of frequencies, and filtering the Fourier spectrum of said upstream signals to limit the spectrum to a band of frequencies at a center frequency that does not interfere with other signals on said shared transmission medium;

and said first node further comprising:

fourth means having an input coupled to receive said upstream clock signal from said first upstream clock generation means and having an input coupled to said shared transmission media and including means for generating a local upstream carrier from said upstream clock signal generated by said first upstream clock generation means which has the same frequency as said upstream carrier generated in each of said second nodes, said fourth means for using said upstream carrier to demodulate upstream signals transmitted by said one or more second nodes to generate demodulated upstream signals, and for recovering said upstream data from said demodulated upstream signals, including using said upstream clock to demultiplex said recovered upstream data [signals] if necessary[prior to recovering the upstream data].

6. (Amended) A modem for use at a headend of a system for bidirectional communication of digital data over a transmission [media] medium, comprising:

a master clock for generating a master clock signal;

means for generating upstream and downstream clock signals which are phase coherent with said master clock signal, said upstream clock signal having a frequency which is M/N times the frequency of said downstream clock signal, where M and N are integers and are not equal;

means coupled to receive said downstream clock signal for using [it] said downstream clock to transmit downstream data over said transmission [media] medium; and

means coupled to receive said upstream clock signal for using [it] said upstream clock to [receive] recover upstream data transmitted over said transmission [media] medium.

7. (Amended) A modem for use as a remote node in a bidirectional communication system having a headend and a plurality of remote nodes coupled to said headend by a transmission [media] medium, comprising:

first means for recovering a downstream clock which is phase coherent with a master clock in said headend from data transmitted by said headend over said transmission media and for using said recovered downstream clock to recover said downstream data;

second means for using said recovered downstream clock to generate an upstream clock which is phase coherent with said recovered downstream clock,

said upstream clock having a frequency which is M/N times the frequency of said downstream clock, where M and N are integers and are not equal; and

third means for using said upstream clock to transmit upstream data from a plurality of different sources to said headend over said transmission [media] medium.

8. The apparatus of claim 7 wherein said third means includes means for transmitting data upstream using synchronous code division multiplexing.

9. The apparatus of claim 7 wherein said third means includes means for transmitting data upstream using time division multiple access multiplexing.

10. The apparatus of claim 7 wherein said third means includes means for transmitting data upstream using DMT multiple access multiplexing.

11. The apparatus of claim 7 wherein said third means includes means for transmitting symbol data upstream using synchronous code division multiplexing by mapping minislots assigned to said modem to one or more symbols and one or more spreading codes.

12. The apparatus of claim 7 wherein said third means includes means for transmitting symbol data upstream using DMT multiplexing by mapping minislots assigned to said modem to one or more symbols and one or more frequencies.

13. (Amended) A modem for use as a remote node in a bidirectional communication system having a headend and a plurality of remote nodes coupled to said headend by a transmission [media] medium, comprising:

first means for recovering a downstream clock from data transmitted by said headend over said transmission [media] medium and for using said recovered downstream clock to generate a local downstream carrier that is of the same frequency and phase coherent with a master clock in said headend and with the downstream carrier used by said headend to transmit said downstream data, and for using said local downstream carrier and said recovered downstream clock to recover downstream data transmitted by said headend;

a clock for generating an upstream clock signal from said recovered downstream clock so as to be phase coherent with said master clock and having a different frequency than said recovered downstream clock and related to the frequency of said downstream clock by the relationship $M/N * F_{ds}$ where F_{ds} is the frequency of said recovered downstream clock and M and N are integers which are not equal; and

third means for using said upstream clock signal to generate an upstream carrier signal and using said upstream clock and upstream carrier signals to transmit upstream data to said headend over said transmission [media] medium.

14. The apparatus of claim 13 wherein said third means includes means for transmitting symbol data upstream using synchronous code division multiple access multiplexing by mapping minislots assigned to said modem to one or more symbols and

one or more spreading codes.

15. The apparatus of claim 13 wherein said third means includes means for transmitting symbol data upstream using DMT multiplexing by mapping minislots assigned to said modem to one or more symbols and one or more frequencies.

16. (Amended) The apparatus of claim 14 further comprising means for [selectably] selectively altering the mapping.

17. (Amended) The apparatus of claim 15 further comprising means for [selectably] selectively altering the mapping.

18. (Amended) A modem for use as a remote node in a bidirectional communication system having a headend and a plurality of remote nodes coupled to said headend by a transmission [media] medium, comprising:

first means for recovering a downstream clock from data transmitted by said headend over said transmission [media] medium and for using said recovered downstream clock to recover downstream data;

a clock means for generating an upstream clock signal from said recovered downstream clock so as to be phase coherent with a master clock in said headend and which has a frequency which M/N times the frequency of said recovered downstream clock where M and N are integers; and

third means for using said upstream clock signal to transmit upstream data to said headend over said transmission [media] medium, and

wherein upstream data transmission is on the basis of assigned minislots counted by a minislot counter in the headend, said minislot counter having a rollover value that defines a superframe boundary, and further comprising ranging means for carrying out the communications of a ranging algorithm to determine an RU frame alignment offset value for a symbol counter to achieve frame synchronization, said symbol counter also having [which also has] a rollover value which defines a superframe of symbols which exactly corresponds in duration with said superframe of minislots, said symbol counter being implemented by said third means, said offset being of a value which will cause . . frame synchronization such that transmission of symbol data upstream occurs with timing such that [the superframe boundaries of] if a superframe of symbols were to be transmitted upstream, the superframe of symbols would arrive at said headend with the frame boundaries of said superframe of symbols aligned in time with said superframe boundaries of said superframe of minislots but wherein actual transmission of upstream symbols occurs only during assigned minislots.

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19. The apparatus of claim 18 wherein said headend sends sync messages and UCD messages downstream, each said sync message carrying a timestamp sample from a timestamp counter in said headend and each said UCD message containing a timestamp at the time of a kiloframe or superframe boundary occurring at said headend, and further comprising means in said modem for calculating an initial offset value from a sync message and a UCD message and for using said offset as an initial offset value or starting point for said ranging means.

20. (Amended) A system for bidirectional communication of digital data between a CU modem and a plurality of RU modems, comprising:

a shared transmission [media] medium coupling said CU and RU modems; and

a CU modem comprising:

a master clock for generating a master clock signal;

first means for generating downstream clock signals;

second means coupled to said shared transmission [media] medium for receiving said downstream clock signal and for using it to transmit downstream data over said shared transmission [media] medium; and

third means coupled to said shared transmission [media] medium [and] for receiving upstream data transmitted over said shared transmission [media] medium and recovering an upstream clock and carrier therefrom and using said recovered upstream clock and carrier signals to demodulate and demultiplex SCDMA multiplexed upstream symbols having their spectrums spread with a plurality of spreading codes, said symbols and spreading codes being mapped to minislots assigned by said CU modem to said RU modem(s); and

an RU modem comprising

fourth means coupled to said shared transmission medium, for recovering a downstream clock and downstream carrier from data transmitted by said CU modem over said shared transmission [media] medium and for using said recovered downstream clock and carrier to recover downstream data including said minislot assignments transmitted from said CU modem;

a timebase for generating an upstream clock and upstream carrier;

fifth means coupled to said shared transmission [media] medium and to said timebase and to said fourth means for mapping said [minslot] minislot assignments to one or more symbols and one or more spreading codes or DMT frequencies for use in transmitting symbols upstream to said CU modem, and for using said upstream clock, said upstream carrier, and said symbols and spreading codes or DMT frequencies mapped to said minislot assignment to transmit upstream data and preamble data to said CU modem over said shared transmission [media] medium.

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9 21. (Amended) A system for bidirectional communication of digital data between a CU modem and a plurality of RU modems, comprising:

a shared transmission [media] medium coupling said CU and RU modems; and

a CU modem comprising:

a master clock for generating a master clock signal;

first means for generating upstream and downstream clock signals which are phase coherent with said master clock signal, said upstream clock signal having a frequency which is M/N times the frequency of said downstream clock signal, where M and N are integers;

second means coupled to said shared transmission [media] medium for receiving said downstream clock signal and for using it to transmit downstream data over said shared transmission [media] medium; and

third means coupled to said shared transmission [media] medium and coupled to receive said upstream clock signal and using it to receive upstream data transmitted over said shared transmission [media] medium; and

an RU modem comprising

fourth means coupled to said shared transmission medium, for recovering a downstream clock from data transmitted by said CU modem over said shared transmission [media] medium and for using said recovered downstream clock to recover downstream data;

fifth means for using said recovered downstream clock to generate an upstream clock which is phase coherent with said downstream clock, said upstream clock having a frequency which is M/N times the frequency of said downstream clock, where M and N are integers; and

sixth means coupled to said shared transmission [media] medium for using said upstream clock to transmit upstream data and preamble data to said CU modem over said shared transmission [media] medium.

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22. (Amended) A system for bidirectional communication of digital data between a CU modem and a plurality of RU modems, comprising:

a shared transmission [media] medium coupling said CU and RU modems; and

a CU modem comprising:

a master clock for generating a master clock signal;

first means for generating upstream and downstream clock and carrier signals which are phase coherent with said master clock signal, said upstream clock signal having a frequency which is M/N times the frequency of said downstream clock signal, where M and N are integers;

second means coupled to said shared transmission [media] medium for receiving said downstream clock signal and said downstream carrier and for

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using them to transmit downstream data over said shared transmission [media] medium; and

third means coupled to receive upstream signals transmitted over said shared transmission [media] medium and coupled to receive said upstream clock signal and said upstream carrier signal and using them in addition to preamble data transmitted by each RU modem to demodulate and demultiplex SCDMA multiplexed upstream symbols in said upstream signals, said symbols having their spectrums spread with a plurality of spreading codes, said symbols and spreading codes being mapped to minislots assigned by said CU modem to said RU modem(s) for upstream transmissions; and

an RU modem comprising

fourth means coupled to said shared transmission medium, for recovering a downstream clock from data transmitted by said CU modem over said shared transmission [media] medium and for using said recovered downstream clock to generate a downstream carrier which is phase coherent with said downstream carrier signal used by said second means to transmit said downstream data and using said downstream clock and carrier signals to demodulate and recover downstream data including said minislot assignment for upstream transmission;

fifth means for using said recovered downstream clock to generate an upstream clock and an upstream carrier which are both phase coherent with said recovered downstream clock, said upstream clock having a frequency which is M/N times the frequency of said downstream clock, where M and N are integers; and

sixth means coupled to said shared transmission [media] medium

including ranging means for establishing frame synchronization, said sixth means for using said upstream clock and upstream carrier signals to transmit upstream symbol data to said CU modem over said shared transmission [media] medium by mapping said [minslot] minislot assignment received from said CU modem to one or more symbols and one or more spreading codes or DMT frequencies for use in transmitting symbols upstream to said CU modem, and for using said upstream clock and upstream carrier and said symbols and spreading codes or DMT frequencies mapped to said minislot assignment to transmit upstream data as well as known preamble data to said CU modem over said shared transmission [media] medium.

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23. (Amended) The apparatus of claim 22 wherein said CU modem [includes] further comprises a minislot counter which rolls over at a programmable count value which defines a superframe boundary, and further comprises a timestamp counter, a timestamp sampler and a sync message generator means for generating sync messages that contain samples taken by said timestamp sampler of said timestamp counter [from time to time] at predetermined times, and for generating UCD messages which contain samples taken by said timestamp sampler of said timestamp counter at superframe boundaries, and wherein said second means transmits said sync messages and UCD messages downstream to said RU modem, and wherein said ranging means of said RU modem includes a symbol counter [coupled to or part of said sixth means] which counts symbols in a superframe of upstream symbols that exactly corresponds in duration to said superframe of [minslot] minislots and which rolls over at a count corresponding to a boundary of a superframe of upstream symbols, and wherein said fourth means

includes offset calculation means for using said sync messages and UCD messages to calculate an offset to load into said symbol counter such that the superframe boundaries of a superframe of said upstream symbols transmitted [upstream] by said sixth means will be approximately superimposed in time at said CU modem with the superframe boundaries of a superframe of minislots mapped to said superframe of symbols.

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24. (Amended) The apparatus of claim 23 wherein said [sixth means further comprises] ranging means of said sixth means achieves frame synchronization more quickly by [for] using said offset calculated by said offset calculation means as a starting point to carry out a trial and error ranging process to determine an exact offset for said symbol counter which will cause said superframe boundaries of a superframe of upstream symbols to be exactly superimposed in time at said CU modem with the superframe boundaries of a superframe of minislots mapped to said superframe of symbols.

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25. (Amended) The apparatus of claim 22 wherein said CU modem includes a minislot counter which rolls over at a count value which defines a superframe boundary, and wherein said RU modem includes a symbol counter coupled to or part of said ranging means of said sixth means which counts symbols in a superframe of symbols that exactly corresponds in duration to said superframe of [minslot] minislots and which rolls over at a count corresponding to a boundary of a superframe of symbols, and wherein said [sixth means further comprises] ranging means [for determining] functions to use a trial and error delay process to determine an exact offset for said symbol counter which will cause said superframe boundaries of a superframe of upstream symbols to be

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exactly superimposed in time at said CU modem with the superframe boundaries of a superframe of minislots mapped to said superframe of symbols.

26. The apparatus of claim 24 wherein downstream data arrives at said second means in the form of packets with headers and wherein said second means further breaks down said packets and headers into FEC frames having overhead bits and ECC error detection and correction bits therein, and wherein said second means includes means for inserting said sync messages and said UCD messages in the stream of downstream data so as to have low jitter by monitoring the point of insertion of every sync or UCD message into every packet based upon the length of the data and header portions of the packet and the length of said sync or UCD message and changing the point of insertion whenever said sync message or UCD message would not fit completely within the data portion of a packet and would straddle a header portion, and by always inserting the sync message or UCD message at the same point in every FEC frame such that whatever straddles of overhead or ECC bits exist are always the same.

27. (Amended) The apparatus of claim 22 further comprising a clock slip detector means coupled to receive said recovered downstream clock and said upstream clock [and] for counting and storing the count of the clock cycles of said upstream clock over each predetermined interval of said recovered downstream clock and generating an interrupt signal at the end of every interval.

28. The apparatus of claim 27 further comprising means for receiving said interrupt signal and for retrieving the count of upstream clock cycles in response

thereto and comparing said count to a predetermined expected number, and if there is a mismatch of more than a predetermined number of clock cycles, for causing said sixth means to cease transmitting.

29. (AMENDED) A process for transmitting data in both directions in a bidirectional digital data communication system having a headend modem and at least one remote modem coupled to said headend modem by a communication medium, comprising:

generating a master clock signal in a headend modem, and generating a downstream clock and carrier signal from said master clock signal both of which are phase coherent therewith, and generating [an] upstream clock and carrier signals in said headend modem from ~~said master~~ clock signal both of which are phase coherent therewith, said upstream clock signal having a frequency which is M/N times the frequency of said downstream clock, where M and N are integers;

transmitting data downstream to a remote modem using said downstream clock and carrier signals;

in said remote modem, recovering at least said downstream clock signal and using it to recover downstream data, and using said recovered downstream clock signal to generate an upstream clock signal and an upstream carrier signal both of which are phase coherent with the recovered downstream clock signal, said upstream clock signal having a frequency which is M/N times the frequency of said recovered downstream clock signal;

achieving frame synchronization;

using said upstream clock and carrier signals to transmit symbol data and known preamble data from said remote modem upstream to [a] said headend

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modem;

using said upstream clock and carrier signals generated in said [head end] headend modem and said preamble data transmitted by said remote modem to recover upstream data transmitted from said remote [node] modem.

30. (Amended) A process for mapping upstream symbols and spreading codes in an SCDMA system to upstream assigned minislots comprising:

organizing data to be transmitted into frames comprised of subframes each of which contains chips generated from symbols in an information vector, with one information vector mapped to each subframe, and a programmable number of frames mapped to every minislot;

counting minislots with a minislot counter that rolls over at some number which defines a superframe of minislots;

setting a rollover count of a symbol counter to establish a superframe of symbols such that if said minislot counter and said symbol counter simultaneously started counting from zero, both would roll over simultaneously;

mapping symbols and spreading codes to minislots by starting on a first code and assigning numbers to symbols to each frame in accordance with how many subframes there are in said frame and continuing this process with subsequent frames along a time axis until a programmable value of L is reached where L is an integer, then repeating the process starting with another code along a code axis and starting with another frame until L is reached again and repeating this process until the number of symbols in a superframe of symbols have been mapped to specific frames and minislots and specific codes.

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31. A process of transmitting SCDMA data in an upstream organized as numbered minislots, comprising:

receiving a minislot assignment naming specific numbered minislots on which transmission is authorized;

mapping the specific minislot numbers in said assignment to specific symbols and spreading codes and frame and subframes that map to those minislots;

constructing one information vector for every subframe mapped to the minislot assignment by placing the numbered symbols that map to the numbered minislots in the assignment in the elements of the information vectors corresponding to the numbered code each numbered symbol maps to;

spreading the spectrum of each information vector by matrix multiplication of the information vector times a code matrix having a plurality of codes therein which corresponds to the number of elements in the information vector to generate one result vector for every subframe that maps to the assigned minislots; and

transmitting RF signals derived from the result vectors.

Please add a new claim 32 as follows:

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32. A modem for use as a remote node in a bidirectional communication system having a headend and a plurality of remote nodes coupled to said headend by a transmission medium, comprising:

first means for recovering a downstream clock which is phase coherent

with a master clock in said headend from data transmitted by said headend over said transmission medium and for using said recovered downstream clock to generate a local downstream carrier which is phase coherent with a downstream carrier that downstream data was modulated on at said headend and which lies in a downstream band of frequencies, said first means for using said recovered downstream clock and local downstream carrier to recover said downstream data;

second means for using said recovered downstream clock to generate an upstream clock which is phase coherent with said recovered downstream clock, said upstream clock having a frequency which is M/N times the frequency of said downstream clock, where M and N are integers; and

third means for using said upstream clock to generate an upstream carrier which is in a different, non-interfering frequency band from the frequency band of said recovered downstream carrier, and for using said upstream clock and said upstream carrier to transmit upstream data from a plurality of different sources to said headend over said transmission medium simultaneously with recovery by said first means of said downstream data, separation of upstream data from said different sources being accomplished using any known form of multiplexing and separation of said transmissions of upstream data from recovery of said downstream data being accomplished by virtue of frequency division multiplexing.

Please add a new claim 33 as follows:

33. A modem for use at a headend of a system for bidirectional communication of

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digital data over a transmission medium, comprising:

a master clock for generating a master clock signal;

means for generating upstream and downstream clock signals which are phase coherent with said master clock signal, said upstream clock signal having a frequency which is M/N times the frequency of said downstream clock signal, where M and N are integers and are not equal;

means coupled to receive said downstream clock signal for using said downstream clock to generate a downstream carrier and use said downstream clock and downstream carrier to transmit downstream data over said transmission medium; and

means coupled to receive said upstream clock signal for using said upstream clock to generate an upstream carrier of the same frequency as the upstream carrier used by remote transceivers to transmit upstream data to said headend transceiver and for using said upstream clock and said upstream carrier and preamble data transmitted by each said remote unit modem to recover upstream data transmitted over said transmission medium.

Please add new claims 34 and 35 as follows:

21 34. A process for bidirectional communication of digital data in a communication system having a headend modem and at least one remote modem coupled to said headend modem by a communication medium, comprising:

generating a master clock signal in said headend modem, and generating a downstream clock and carrier signal from said master clock signal both of which are phase coherent therewith, and generating upstream clock and carrier signals in said headend modem from said master clock signal both of which are phase

coherent therewith, said upstream clock signal having a frequency which is M/N times the frequency of said downstream clock, where M and N are integers;

transmitting data downstream to a remote modem using said downstream clock and carrier signals; and

using said upstream clock and carrier signals and known preamble data transmitted by each said remote unit modem to recover upstream data transmitted by each of said remote unit modems.

Alt Cont.

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35. The process of claim 34 further comprising the steps of using a timestamp counter to count the ticks of a timestamp clock which may or may not be said master clock in said headend, and periodically sampling said timestamp counter and periodically generating synchronization messages and transmitting said synchronization messages as part of said downstream data with no more than 200 milliseconds between adjacent synchronization messages, and sampling said timestamp counter each time an upstream kiloframe boundary is detected in said upstream data and generating and transmitting a UCD messages as part of said downstream data from time to time with each UCD message containing a sample of said timestamp counter at an upstream kiloframe boundary of said headend modem, each synchronization message containing the count of said timestamp counter.

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36. A process for bidirectional communication of digital data in a communication system having a headend modem and at least one remote modem coupled to said headend modem by a communication medium, comprising:

in said remote modem, receiving downstream transmissions from said

headend modem and recovering a downstream clock signal from said downstream transmissions and generating a local downstream clock and a downstream carrier from said recovered downstream clock, both said local downstream clock and said downstream carrier being phase coherent with said recovered downstream clock;

using said local downstream clock and said downstream carrier to recover downstream data;

using said recovered downstream clock signal to generate an upstream clock signal and an upstream carrier signal both of which are phase coherent with the recovered downstream clock signal, said upstream clock signal having a frequency which is M/N times the frequency of said recovered downstream clock signal;

achieving frame synchronization using a ranging process;

using said upstream clock and upstream carrier signals to transmit symbol data and known preamble data from said remote modem upstream to said headend modem.

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37. The process of claim 36 further comprising the steps:

(1) establishing an initial upstream kiloframe boundary in said remote modem;

(2) counting ticks of said upstream clock in a local kiloframe counter and resetting said counter to zero at the beginning of each new upstream kiloframe;

(3) sampling the count of said local kiloframe counter each time a synchronization message is received;

(4) detecting when a synchronization message is received in said

downstream data and when a UCD message is received in said downstream data and extracting timestamp data from each;

(5) determining the number of local kiloframe counter clock cycles in N frames where N is the number of upstream frames in the interval between the time that an upstream kiloframe marker is received at said headend modem minus the downstream propagation delay between this remote unit modem and said headend modem;

(6) using a timebase conversion factor between a clock frequency that drives a timestamp counter in said headend modem and said upstream clock being counted by said local kiloframe counter and the timestamp data extracted in step (4) and the data calculated in step (5) to calculate an offset value;

(7) using said offset value to speed up the ranging process to achieve frame synchronization.

Please add a new claim 38 as follows:

25 38. A process of achieving frame synchronization in a remote modem in a bidirectional digital data communication system having a headend modem that transmits MCNS downstream data to one or more remote unit modems coupled to said headend modem by a shared communications medium, comprising:

waiting for said remote unit modem to achieve clock synchronization with a master clock in said headend modem by recoving a downstream clock from transmissions from said headend modem and using said recovered downstream clock to generate a local downstream clock and a local upstream clock, both of which are phase coherent with said master clock in said headend modem;

establising an initial arbitrary upstream kiloframe boundary;

waiting to receive at least one synchronization message and one UCD message in said remote unit modem from said headend modem;

computing an upstream kiloframe boundary adjustment using timestamp data in said synchronization and UCD messages;

waiting for at least one upstream kiloframe to pass and performing a ranging process using said upstream kiloframe boundary adjustment value to determine an upstream transmission delay value TD to achieve precise kiloframe boundary frame synchronization; and

storing the value of TD in memory and using it for subsequent upstream kiloframe transmissions by said remote unit modem.